REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-2 and 4-17 are presently active in this case, Claims 1-2, 4-5, 10-11, and 14-17 are amended and Claim 3 has been canceled by way of the present amendment.

In the outstanding Office Action, Claims 4, 6, 10, 11, 14-17 were objected to for informalities; Claims 1-3, 5, 8-9 and 12-13 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 2, 5, and 12-13 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,333,857 to Kanbe et al.; Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al.; and Claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. in view of U.S. Patent No. 6,323,435 to Strandberg.

With regard to the certified copy of the priority document, Applicants note that a request was made to the Japanese patent office to forward this document to the USPTO. Applicants respectfully request that the examiner inquire as to whether the document was received.

With regard to the objection to the claims, Applicants have amended the claims herein to eliminate improper multiple dependent claim format. Therefore the objection to the claims is believed to be overcome. Further, the claims are amended herein to correct discovered informalities and to clarify the claimed invention.

With regard to the rejection under 35 U.S.C. § 112, second paragraph, Applicants have amended the claims to correct informalities noted in the outstanding Office Action. Therefore, the rejection under 35 U.S.C. § 112, second paragraph, is believed to be overcome.

Turning now to the merits, in order to expedite issuance of a patent in this case, Applicants have amended independent Claim 1 to clarify the patentable features of the present invention over the cited references. Specifically, Applicants' Claim 1, as amended, recites a multi-layer printed wiring board including a core substrate having a plurality of through holes therein, the through holes in the core substrate being disposed so that a ground through hole and a power through hole adjoin each other and a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm. An interlayer insulating layer is formed on the core substrate, and a conductive layer is formed on the interlayer insulating layer. A plurality of via holes are provided in the insulating layer and configured to provide electrical connection between the conductive layer and through holes.

Thus, Claim 1 has been amended to recite that a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm. As discussed in Applicants' specification, an IC chip utilizing high switching frequency (for example 5GHz) is prone to switching errors. However, when loop inductance of the printed circuit board for mounting the IC chip is lower than 60pH, IC chip errors can be reduced. Based on this fact, the present inventor conducted studies and experiments to determine a relationship between loop inductance and distance between the ground through hole and power through hole. Based on such research, the inventor discovered that a distance between ground and power through holes of 60 to 550 μm can provide desired loop inductance and therefore reduce switching errors, even at high switching speeds of 3Ghz or more. Data relating to these experiments is shown in Fig. 16.

In particular, as discussed in Applicant's specification, "[i]f it is less than 60 μm, any insulating gap cannot be secured between the through holes, thereby causing such a fault as short-circuit. Due to an insulating gap or the like, it can be difficult to set the loop inductance

within the range of a design permissible value."[1]. Further, "[b]y disposing the ground through hole adjacent to the power through hole, induced electromotive forces cancel out each other because the directions of the induced electromotive forces are opposite."[2] However, when the distance is longer than 550 μm, the effect of the cancellation of the induced electromotive forces is reduced, and the loop inductance increases. As the result, power supply to the IC chip is delayed, signal delay may occur. This discovery of a range of distance between the ground and power through holes was made by the inventor.

The cited reference to Kanbe et al. discloses a printed wiring board having a laminated capacitor consisting of composite dielectric layers and metal layers alternately laminated. A first set of metal layers electrically connected to form a first electrode of the capacitor is connected to a first through-hole, while a second set of metal layers electrically connected to form a second electrode of the capacitor is connected to a second through-hole. The first through-hole and first electrode are connected to ground, while the second through-hole and electrode are connected to power. Thus, in Kanbe et al., the laminated capacitor is parallel inserted between the power source voltage and the land voltage such that noise can be suppressed.

That is, Kanbe et al. utilizes the laminated capacitor in the core substrate to solve the problem of noise or delay of power supply to the IC chip which causes switch errors. Therefore, there is no need in Kanbe et al. to provide a particular distance requirement between the power and ground through holes. Thus, Kanbe et al. clearly does not show or suggest any particular distance range between the power and ground through holes. Indeed, since Kanbe et al. forms a laminated capacitor in the core substrate, if the distance between the through-holes is reduced, an effective area of the capacitor electrode (area of the metal

[1] Applicant's specification at page 6 lines 5-10.
[2] Applicant's specification at page 3 lines 16-19.

layer between adjoin through-hole) is reduced. This would create a problem of reduced capacitance in Kanbe et al.

Strandberg is cited for features of the dependent claims and does not show the distance between the through hole, and placement of the ground through hole and the power through hole. Therefore, Strandberg does not correct the deficiencies of Kanbe et al.

Thus, even if Kanbe and Strandberg are combined, this combination would not result in "through holes in the core substrate being disposed so that a ground through hole and a power through hole adjoin each other, wherein a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm" as recited in Claim 1. Thus, Claim 1 patentably defines over the cited references. As the remaining Claims depend from Claim 1, these claims also patentably define over the cited references.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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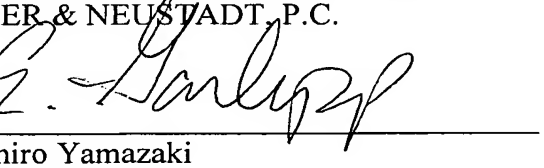

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